# Lab 2 Structural Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? \_yes\_\_

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here. Otherwise write “n/a”: **\_n/a\_\_\_**

Student Name: Chris Cyr  
Student ID: 12436037  
Date Completed: 5/5/22  
Time Spent: Reviewing Digital Design Material: 20 min  
 Design/Preparation Work: 6 hours (I shouldn’t have k-mapped it)  
 VHDL Coding & Debugging: 4 hours

## Structural Overview

What % do you feel you completed on the lab? Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

\_100%\_\_\_

## Lab 2 Truth Table(s)

Create a truth table showing **Permit**, **ReturnChange**, and **NextState** based on your FSM. You can use Word, Excel, or even attach a picture of your truth table as long as it is legible. It must be in the correct orientation & legible for full credit.



**Permit** = **C3C2’**

**ReturnChange** = **C3C0**

**NextState3 = I0C3'C2C1C0 + I1C3'C2C0 + I2C3'C0 + I2I1'C3'C2'C1'**

**NextState2 = I2'I1'I0'C3'C2 + C2C0' + I0C3'C2'C0 + I2'I1'C3'C1'C0 + I2'I1C3'C1'C0' + I1C3'C2'C0 + I1I0C3'C0**

**NextState1 = I2'I1'I0'C3'C1 + C1C0' + I2'I0C3'C2'C0' + I0C3'C1'C0 + I2'I0'C3'C2'C0 + I1I0C3'C0**

**NextState0 = I2C0 + I2'I1'I0'C3'C1 + I2'I1'I0'C3'C2 + I0C3C0 + I0'C3'C2C1C0 + I1C3C0**

Explain any optimizations you may have made to your equations here.

I put them through a K-map to simplify

## Lab 2 Minimum Clock Cycle

Minimum clock cycle: \_10.6\_ ns

Explain how you derived your minimum clock cycle (as discussed in EECS 31) here.

5.6ns delay for equations, 4ns clock delay, 1ns setup time

## Lab 2 Structural Simulation Graph

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

A screenshot of a computer

Description automatically generated with medium confidence

## Lab 2 Structural and Behavioral Simulation Graph Comparisons

Compare your behavioral & structural graphs here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

SA screenshot of a computer

Description automatically generated with medium confidence

BA screenshot of a computer

Description automatically generated with medium confidence

The structural one had delays but otherwise they looks exactly the same